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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,050	02/14/2002	Stephen R. Cebenko	1-1-3-1-1	9454

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EXAMINER	
NGUYEN, DAO H	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,050	CEBENKO ET AL.	
	Examiner	Art Unit	
	Dao H Nguyen	2818	

-- Th MAILING DATE of this communication app ars on th cov r sh et with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In response to the communications dated 02/14/2002 through 09/19/2003, claims 1-18 and 20 are active in this application as a result of the addition of claims 20 and the cancellation of claims 19.

Information Disclosure Statement (IDS)

2. No Information Disclosure Statement (IDS) has been filed in this application.

Acknowledges

3. Applicant made a provisional election without traverse to prosecute the invention of Group I, claims 1-18, drawn to a semiconductor device. Affirmation of this election was made in the Response to Restriction Requirement filed 09/19/2003, and made of record as Paper filed 0903.

Claim 19 has been cancelled due to non-elected Group.

New claim 20 has been added.

Specification

4. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim(s) 1-18 is/are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 18, the limitations, "the first and second gates each extending longitudinally along a first axis from a first end adjacent one of the source and drain regions to a second end **extending past another of the source and drain regions**" is not clearly defined and distinctly pointed out the subject matter which is claimed as the Applicant's invention. The phrase "extending past another of the source and drain regions" is not understood. Is the gate extending past over one of the source and drain region? If so, then does it extend outside of the active channel region defined between the source and drain of the transistor? And if so, then how can?

Claim 1-17 depend from rejected claim 1 and include all of the limitations of claim 1, thereby rendering these dependent claims indefinite.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. Claim(s) 1-6, 8-18, and 20 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,461,577 to Shaw et al.

Regarding claims 1 and 20, Shaw discloses a base transistor structure for use in an integrated circuit, as shown in figures 1, 5-8, and 10-11, the base transistor structure comprising:

a plurality of source regions;

a plurality of drain regions, each adjacent to a corresponding one of the source regions; and

at least first and second elongated gates, the first and second gates each overlying a corresponding subset of the source and drain regions, the first and second gates each extending longitudinally along a first axis from a first end adjacent one of the source and drain regions to a second end adjacent another of the source and drain

regions, the first and second gates being separated from one another at the second ends thereof;

the base transistor structure being substantially symmetric about the first axis; and .

the base transistor structure being configured such that multiple ones of the base transistor structure arranged immediately adjacent to one another are utilizable to form one or more circuit cells of the integrated circuit.

See also column 3, lines 23-40, column 18, lines 6-39, and the abstract.

Regarding claim 2, Shaw discloses the base transistor structure wherein the first and second elongated gates are connectable at the second ends thereof by a conductor formed in a metallization layer of the integrated circuit. See figures 6, 8, and 10-11, and column 3, lines 28-34.

Regarding claim 3 Shaw discloses the base transistor structure wherein the first and second gates are associated with respective PFET and NFET devices of the base transistor structure. Note that the logic circuit of Shaw can be formed by either or both of NMOS and PMOS.

Regarding claim 4, Shaw discloses the base transistor structure wherein at least one of the multiple ones of the base transistor structures, arranged immediately

adjacent one another, is configurable to provide gate isolation for active transistors in other ones of the base transistor structures. See figures 6, 8, and 10-11.

Regarding claim 5, Shaw discloses the base transistor structure wherein the first axis corresponds to a y-axis. See figures 6, 8, 10-11.

Regarding claim 6, Shaw discloses the base transistor structure wherein the base transistor structure is substantially symmetric about a second axis perpendicular to the first axis. See figures 6, 8, 10-11.

Regarding claim 8, Shaw discloses the base transistor structure wherein the gates are configured so as to permit crossover routing of interconnects within a given one of the circuit cells. See figures 6, 8, 10-11.

Regarding claim 9, Shaw discloses the base transistor structure wherein metallization layer connections of the integrated circuit are used to form the circuit cells from the multiple ones of the base transistor structure. See figures 6, 8, 10-11.

Regarding claim 10, Shaw discloses the base transistor structure wherein the circuit cells comprise programmable cells of a cell library having a plurality of cells each of which is comprised of multiple ones of the base transistor structure. This is common in the art.

Regarding claim 11, Shaw discloses the base transistor structure wherein a given one of the circuit cells comprises a logic gate formed from a plurality of the base transistor structures. See column 2, lines 16-28.

Regarding claim 12, Shaw discloses the base transistor structure wherein a given one of the circuit cells comprises a flip-flop circuit formed from a plurality of the base transistor structures. This is well known in the art.

Regarding claim 13, Shaw discloses the base transistor structure wherein a plurality of the circuit cells comprise spare gates of the integrated circuit, the spare gates being convertible to active gates using connections formed in a metallization layer of the integrated circuit. See figures 6, 8, 10-11.

Regarding claims 14-17, Shaw discloses the base transistor comprising all claimed limitations. See figures 6, 8, 10-11.

Regarding claim 18, Shaw discloses an integrated circuit, as shown in figures 1, 5-8, and 10-11, comprising:

a plurality of circuit cells, each of al least a subset of the plurality of circuit cells being formed as an interconnection of multiple base transistor structures arranged immediately adjacent to one another;

a given one of the base transistor structures comprising:

a plurality of source regions;

a plurality of drain regions, each adjacent to a corresponding one of the source regions; and

at least first and second elongated gates, the first and second gates each overlying a corresponding subset of the source and drain regions, the first and second gates each extending longitudinally along a first axis from a first end adjacent one of the source and drain regions to a second end adjacent another of the source and drain regions, the first and second gates being separated from one another at the second ends thereof;

the base transistor structure being substantially symmetric about the first axis.

See also column 3, lines 23-40, column 18, lines 6-39, and the abstract.

Claim Rejections - 35 U.S.C. § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim(s) 7 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,461,577 to Shaw et al., in view of the following remarks.

Regarding claim 7, Shaw discloses the base transistor structure comprising all claimed limitations, except for having a width corresponding approximately to a single grid of a standard cell CAD tool. However, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the width of the transistor of Shaw as claimed because those skilled in the art will recognize that such modification and variations involve only routine skills in the art, and can be made without departing from the spirit of the invention of Shaw.

Conclusion

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (703) 305-1957. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308 - 4910. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
October 16, 2003